

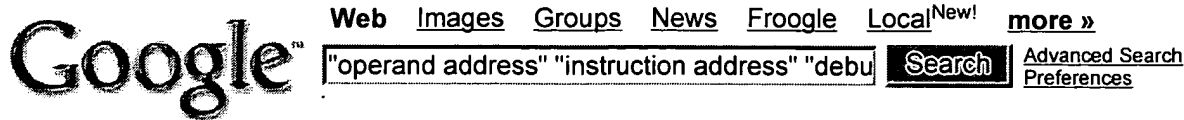
WEST Search History

DATE: Tuesday, November 08, 2005

Hide?	<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>
		<i>DB=PGPB,USPT,USOC; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L28	717/128,129.ccls. and (debug module or debug circuit).ab.	2
<input type="checkbox"/>	L27	717/128,129.ccls. and (debug module or debug circuit or address).ab.	96
<input type="checkbox"/>	L26	L23 and L3	40
<input type="checkbox"/>	L25	L23 and L2	143
<input type="checkbox"/>	L24	L23 and L1	296
<input type="checkbox"/>	L23	L22 or L21 or L20	7946
<input type="checkbox"/>	L22	(714/17 714/18 714/30 714/31 714/32 714/33 714/34 714/35 714/36 714/37 714/38 714/39 714/40 714/41 714/42 714/43).ccls.	5247
<input type="checkbox"/>	L21	(712/32 712/33 712/34 712/35 712/36).ccls.	1081
<input type="checkbox"/>	L20	(717/124 717/125 717/126 717/127 717/128 717/129 717/130 717/131 717/132 717/133).ccls.	2084
<input type="checkbox"/>	L19	717/124-133.ccls	0
		<i>DB=USPT; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L18	L11	35
		<i>DB=EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L17	L16	31
		<i>DB=JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L16	L12 and (information near (trace or debug\$))	44
<input type="checkbox"/>	L15	L12 and (bus near (interfac\$ or link))	7
<input type="checkbox"/>	L14	L12 and ((bus near communication) same processor)	0
<input type="checkbox"/>	L13	L12 and (bus near (interfac\$ or link) same processor)	0
<input type="checkbox"/>	L12	debug\$ near (circuit or chip or module)	475
		<i>DB=USPT,PGPB; PLUR=YES; OP=ADJ</i>	
<input type="checkbox"/>	L11	L10 and exception	61
<input type="checkbox"/>	L10	L9 or L8	135
<input type="checkbox"/>	L9	L1 and (bus near (interfac\$ or link) same processor)	125
<input type="checkbox"/>	L8	L1 and ((bus near communication) same processor)	26
<input type="checkbox"/>	L7	L6 and exception	21
<input type="checkbox"/>	L6	L5 or L4	36
<input type="checkbox"/>	L5	L2 and (bus near (interfac\$ or link) same processor)	35

<input type="checkbox"/>	L4	L2 and ((bus near communication) same processor)	8
<input type="checkbox"/>	L3	L2 and bus near (interfac\$ or link)	73
<input type="checkbox"/>	L2	L1 and information near (trace or debug\$)	270
<input type="checkbox"/>	L1	debug\$ near (circuit or chip or module)	1127

END OF SEARCH HISTORY



Web Results 1 - 10 of about 96 for "**operand address**" "**instruction address**" "**debug module**". (0.72 seconds)

[PDF] Module Introduction

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Debug module (included on all standard parts except MCF5102) ... **Operand Address**.

Generation. Operand Fetch 1. Operand Fetch 2. Execute ...

eelab.sjtu.edu.cn/mot/course/ codefire/summary/..%5Cmodule21037%5Ccores.pdf - [Similar pages](#)

An Embedded Processor Architecture With Extensive Support For SoC ...

Instruction address (IA) and **operand address** (OA) watchpoint channels can each match on a range of ... DM: **Debug module** IA: **Instruction address** (watchpoint) ...

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An Embedded Processor Architecture With Extensive Support For SoC ...

... unit DM: **Debug module** IA: **Instruction address** (watchpoint) IP: Intellectual property

IV: Instruction value (watchpoint) OA: **Operand address** (watchpoint) SOC ...

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used twice: first, for **operand address** generation and sec- ... Fig.4 ColdFire

debug module block diagram, showing real-time and background debug datapaths. ...

www.freescale.com/files/ dsp/doc/white_paper/MCF5XXDBWP.pdf - [Similar pages](#)

[PDF] FreescaleSemiconductor, Inc. ...

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This 32-bit bus connects the core and **debug module** with any on-chip ... The standard execution stage includes an ALU for **operand address** calculations, ...

www.freescale.com/files/ 32bit/doc/white_paper/COLDFIRE3WP.pdf - [Similar pages](#)

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SH-5: The 64-Bit SuperH Architecture

... including **instruction address**, instruction code, **operand address**, ... Through an initiator port on the **debug module**, the external debug host can access ...

doi.ieeecomputersociety.org/10.1109/40.865864 - [Similar pages](#)

EP1089183 St european software patent - Microcomputer debug ...

[0101] A **debug module** 72 containing a debug interface is coupled to system bus

56 via ... For example, if the watchpoint is an **operand address** watchpoint, ...

gauss.ffii.org/PatentView/EP1089183 - 104k - [Cached](#) - [Similar pages](#)

[PDF] COP87L40RJ/COP87L42RJ One-Time Programmable (OTP) Microcontroller ...

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There are ten addressing modes six for **operand address**- ing and four for transfer

of control ... COP8 **Debug Module** Moderate cost in-circuit emulation ...

eshop.engineering.uiowa.edu/NI/pdfs/01/28/DS012862.pdf - [Similar pages](#)

[PDF] Debug Support on the ColdFire Architecture

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... used twice: first, for **operand address** generation and ... the core asserts cpu_wrt_drc in the **debug module**. ... in the calculation of the target **instruction address**. ...

pccorot15.obspm.fr/COROT-ETC/ Files/MCF5282/MCF5XXDBWP.pdf - Supplemental Result - [Similar pages](#)

[PDF architecture](#)

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The on-chip **debug module** contains the debug links and a ... four **instruction-address** range (IA) channels. • two **operand-address** range (OA) channels ...

sft2000.komputilo.org/downloads/sh5_whitepaper.pdf - [Similar pages](#)

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